Multi-code state assignment for low power design

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Abstract: A multi-code state assignment is proposed to realise priority encoding by restraining redundant states. A state assigned with multi-code can be allocated using fewer state variables; further, flip-flops corresponding to those absent state variables can be clock-gated. An algorithm is presented to implement the multi-code state assignment for general sequential circuits. As a result, lower power dissipation may be attained. Practical design examples are simulated by PSPICE and demonstrate that this technique can lead to sizable power savings.

1 Introduction

The direct synthesis of sequential circuits for low power [1-5] is an area of exploration which promises more global power savings. The sequential circuit design can be divided into the following steps: state reduction (for determining the number of state variables), state assignment (for determining the corresponding relation between states and state variable values), choice of flip-flops (the number is equal to that of state variables), and design of the combinational circuit part (for providing outputs and next states). Overall, state assignment has an important role in determining the number of nodes required to implement the output and next logic. On the other hand, state assignment directly affects the switching activity of the state variables and the interior variables in the circuit. We know that both the number of nodes and the switching activity influence the power dissipation of a combinational circuit. From this, we realise that state assignment is the critical step in low power design of a sequential circuit.

During the low power design of combinational circuits we have found that blocking the redundant signals and shutting off the redundant circuit parts is an effective method of lowering energy dissipation. If a certain part of the circuit has no effect on the circuit functionality during some time period, it is called redundant. If this part stops working (by cutting off the power supply or by fixing its input signals), energy saving can be obtained. For the design of sequential circuits this technique of exploiting redundancy can be executed in the low power dissipation corresponding combinational logic parts. Compared with a combinational circuit, however, there are several special design aspects in a sequential circuit:

(i) A sequential circuit has flip-flops which store state signals.

(ii) A sequential circuit has flip-flops which can be clocked

(iii) States are assigned by encoding state variables.

We next describe three restraining techniques with respect to each of these aspects:

(i) Traditional flip-flops are single-edge triggered flip-flops (SEFF), which are sensitive to the rising or falling edge of the clock. So half of the clock's transitions have nothing to do with the circuit and become redundant behaviours, which in turn results in wasteful dynamic energy dissipation in these flip-flops. For this reason a double-edge triggered flip-flop (DETFF) can be used, which utilises both transition edges of the clock, thereby achieving energy saving [6-8].

(ii) The function of the clock is to force all flip-flops to change their state synchronously (present state to next state). During this switching process, if a certain flip-flop's next state is the same as its present state, this flip-flop is in a holding mode. The clock's triggering for it is redundant and can be masked. Therefore a workable clock gating technique was developed to lower the energy dissipation, and it works [9-11].

(iii) In the state assignment, $k$ state variables are used to express $2^k$ different states. However, if the number of working states $l$ is not equal to $2^k$, there will exist $(2^k - l)$ redundant states in state assignment. Of course, these redundant states are beneficial in reducing the complexity of the combinational circuit, but the reliability of the circuit may be influenced. We have to consider the system's behaviour if it enters into one of these redundant states and seek to make the system self-corrective. Theoretically, there should be a technique for avoiding the redundant states, which is useful for saving power, but we have not seen any work in this field up to now.

This paper proposes a multi-code state assignment to avoid encountering redundant states. The result of multi-code state assignment is that some states do not require binary assignment of all state variables. When the system is in such a state, the unused state variables become redundant. From this principle we study the corresponding redundancy restraining technique and consider its availability in the low power design of sequential circuits.
2 Priority encoding by using redundant states

In combinational circuit design, the existence of redundant states is helpful in generating a larger prime implicant during boolean optimisation. If the implicant contains $2^m$ minterms, a maximum of $m$ variables may be reduced in the product-form. If we use $k$ state variables to express $l$ different states ($l \leq 2^k$), there will be $(2^k - l)$ redundant states. In fact, we may change the uni-code state assignment where a state code corresponds to a state variable minterm. The $(2^k - l)$ redundant states may be utilised to make some states multi-coded, such as two-coded, four-coded, etc. These corresponding state assignments are equal to the larger implicants in combinational circuit design, which have fewer state variables. Thus it can be seen that those absent variables are redundant when the system is in these states. Because the corresponding flip-flop outputs are not being used, these flip-flops can be isolated from the clock so as to reduce their dissipation.

A special example of a sequential circuit with many redundant states is the one-hot ring counter, where each state corresponds to a state variable. Take a four-state ($S_1-S_4$) counter as an example. Fig. 1a shows the state assignment Karnaugh map and the state assignment table of the four states corresponding to four state variables ($Q_1-Q_4$). Notice that each state is encoded by a state variable minterm. The result is twelve (12) multi-code state assignment, as shown in Fig. 1b. Although these redundant states can be used to simplify the corresponding circuits $Q_1-Q_4$ can be used to restrain the switching of $Q_1$ and $Q_3$, and $Q_2$ can be used to restrain the switching of $Q_2$. This restraint function can be realised by a clock-gating technique, as shown in Fig. 1c. Notice that the signal for gating the clock to $Q_2$ is $D_1$ rather than $Q_1$. The reason is that when the clock comes, $D_1 = 1$ and hence block the clock to $Q_2$. The energy dissipation waveform of the two circuit in Fig. 2b shows that the three flip-flops work synchronously. Notice that the omitted fourth flip-flop is replaced by a NOR gate in the circuit.

Because $Q = D$, the next state equation of the flip-flop, the exciting functions of the three flip-flops can be derived based on the state table shown in Fig. 2b:

$$D_1 = Q_1 + Q_2 + Q_3, \quad D_2 = Q_1, \quad D_3 = Q_2$$

In Fig. 2b $S_1$ is quad-coded and $S_2$ is double-coded in assignment while $S_3$ and $S_4$ are uni-coded. We found that $Q_1$ has the highest priority which means that if $Q_1 = 1$, the values of other $Q_2, Q_3$ are trivial. Besides, $Q_1$ has the second high priority in three state variables. Therefore in the corresponding circuits $Q_1 = 1$ can be used to restrain the switching of $Q_3$ and $Q_2$, and $Q_3$ can be used to restrain the switching of $Q_2$. The restraint function can be realised by a clock-gating technique, as shown in Fig. 2c. Notice that the signal for gating the clock to $Q_2$ is $D_1$ rather than $Q_1$. The reason is that when the clock comes, $D_1 = 1$ and hence block the clock to $Q_2$. The energy dissipation waveform of the two circuit in Fig. 2b shows that the three flip-flops work synchronously. Notice that the omitted fourth flip-flop is replaced by a NOR gate in the circuit.

The circuit of Fig. 2c has been simulated by PSPICE. Fig. 3a shows waveforms of the three clock signals for the three flip-flops and the four outputs. Three clocks clk1, clk2, clk3 are basically synchronous, and those four outputs $Q_1-Q_4$ prove that this circuit has correct logic functionality.

Now let us discuss the power dissipation in the new design. The state assignment table in Fig. 1a shows that the four flip-flops receive 16 triggering actions from the clock in one cycle. However, the state assignment table in Fig. 2b shows that the three flip-flops receive only nine triggering actions from the clock in one cycle. Consequently, the power saving owing to reducing one flip-flop and gating clock should be $(16 - 9)/16 = 43\%$. The energy dissipation waveform of the two circuit in Fig. 3b shows that the power saving is in fact 33%. The disparity is produced because of the energy dissipation in the NOR gates used for gating clock.

The design of Fig. 2c not only simplifies the circuit construction and saves the energy dissipation but also improves the circuit's reliability because of the nonredundant states. The complete state diagram in Fig. 2b shows this advantage.
3 Determination of multi-code state assignment

The uni-code state assignment corresponds to a minterm of the state variable space. In contrast, the multi-coded state assignment contains \(2^n\) minterms of the state variable space. We have thus utilised or restrained \(2^n - 1\) redundant states. Therefore we can decompose the set of redundant states in groups of \(2^k - 1\) states and determine the corresponding multi-code state assignment. In the last Section, there were 12 redundant states when four state variables \(Q_1 - Q_4\) were used. The nonredundant state assignment in Fig. 2b is achieved. Evidently, the inclusion of redundant state in state assignment increases the complexity of the assignment procedure. We can, however, modify it on the basis of single-code assignment. This method both simplifies the procedure and maintains some characteristics of the original design. We take two sequential circuits in common use as examples to discuss the state assignment algorithm.

3.1 Example 1: Decimal up-counter

In this counter, ten counting states (0, 1, … 9) are encoded with the conventional 8421 BCD encoding, as shown in the left of Table 1. Notice that there are six redundant states in this encoding: \(\{1010, 1011, 1100, 1101, 1110, 1111\}\). From the Table, the excitation functions for the four flip-flops can be derived as

\[
\begin{align*}
D_D &= CBA + D\bar{A} \\
D_C &= CB + CA + \bar{C}BA \\
D_B &= DBA + B\bar{A} \\
D_A &= \bar{A}
\end{align*}
\]

Now we discuss the multi-code assignment by using six redundant states. Since \(6 = 3 + 3\), two states among ten digits can be quad-coded. Analysing the original 8421 BCD state encoding table, both states 9 and 10 can be quad-coded, as shown in the right of Table 1. This new scheme maintains the original characteristics. As \(D = 1\) can be used to restrain state variables \(C\) and \(B\), the priority of \(D\) is higher than \(C\) and \(B\). In a practical circuit, the output 1 of flip-flop \(D\) can be used to isolate the clock to trigger flip-flop \(C\) and flip-flop \(B\) so as to reduce the corresponding energy dissipation. It is not difficult to get the new excitation functions of four flip-flops:

\[
\begin{align*}
D_D &= DBA + D\bar{A} \\
D_C &= DC + DBA \\
D_B &= DBA + B\bar{A} \\
D_A &= \bar{A}
\end{align*}
\]

Comparison between eqns. 1 and 2 shows that \(D_B\) and \(D_A\) are the same in both sets. However, in the latter design, a literal \(\bar{D}\) is added to \(D_P\), and the form of \(D_C\) is simplified. The result is that the combinational circuit part is simpler, and the power dissipation is lower. As to the energy dissipation of flip-flops, the occurrence probability of each state in one cycle is 10%. From the right part of Table 1, as flip-flops \(C\) and \(B\) are restrained in states 8 and 9, they save 20% energy dissipation for themselves. As to all four flip-flops, the energy dissipation saving is 10%. Furthermore, the extra clock gating NOR gate leads to some additional energy dissipation.

Table 1: Encoding of decade up-counter

<table>
<thead>
<tr>
<th>Digit</th>
<th>D</th>
<th>C</th>
<th>B</th>
<th>A</th>
<th>D</th>
<th>C</th>
<th>B</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

In these examples, the occurrence probability of each state was the same. In a general sequential circuit, however, each state’s probability is not the same. To obtain the maximum power saving, a state with higher occurrence probability should be encoded first. The following algorithm will produce a multi-code state assignment for the low power design based on the above example.

Algorithm 1: Given an initial state assignment scheme \(S_A\) for a sequential machine with a state set \(S\) and a redundant state set \(R_S\), the following steps will produce a multi-code state assignment with the low power dissipation:

Step 1: If \(R_S\) is empty, return \(S_A\) and exit. Otherwise, let \(S_{A\text{temp}}\) be \(S_A\) and compute the occurrence probabilities of all the states in \(S\) based on the state table. Then sort the states in descending order of probability.

Step 2: For the first state \(s'\) with the highest probability in \(S\), select a cube \(c\) as large as possible that covers \(s'\) and other redundant states, but not any other states in \(S\). Hence
s' is assigned with multi-codes covered by c. Then remove the redundant states covered by cube c from RS. Repeat this procedure for the next state until there is no remaining state in S or no redundant state left in RS.

Step 3: Suppose the state assignment scheme obtained in step 2 is SA1. Update SAtemp with SA1 if its corresponding circuit needs less power dissipation. Then go to step 2 until there is no alternative selection of cubes for each state in S. This cube selection operation can be handled efficiently by the procedures proposed in ESPRESSO [13]. Update SAtemp each time when a better scheme is found.

Step 4: If SAtemp and SA0 are different, replace SA0 with SAtemp and go to step 1 with updated redundant state set RS; otherwise, go to step 5.

Step 5: Return SAtemp as the final multi-code state assignment scheme.

**Table 2: State of corrector**

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
<th>Output R</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0</td>
<td>T=0</td>
<td>T=0</td>
</tr>
<tr>
<td>A</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>B</td>
<td>C</td>
<td>D</td>
</tr>
<tr>
<td>C</td>
<td>E</td>
<td>F</td>
</tr>
<tr>
<td>D</td>
<td>F</td>
<td>F</td>
</tr>
<tr>
<td>E</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>F</td>
<td>A</td>
<td>A</td>
</tr>
</tbody>
</table>

**Table 3: State assignment**

<table>
<thead>
<tr>
<th>State</th>
<th>Scheme 1</th>
<th>Scheme 2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x  y  z</td>
<td>x  y  z</td>
</tr>
<tr>
<td>A</td>
<td>0  0  0</td>
<td>φ  0  0</td>
</tr>
<tr>
<td>B</td>
<td>0  0  1</td>
<td>φ  0  1</td>
</tr>
<tr>
<td>C</td>
<td>1  1  1</td>
<td>1  1  1</td>
</tr>
<tr>
<td>D</td>
<td>0  1  1</td>
<td>0  1  1</td>
</tr>
<tr>
<td>E</td>
<td>1  1  0</td>
<td>1  1  0</td>
</tr>
<tr>
<td>F</td>
<td>0  1  0</td>
<td>0  1  0</td>
</tr>
</tbody>
</table>

### 3.2 Example 2: 8421 BCD detector

An 8421 BCD detector receives a serial entry T, and four bits as a group (the less significant bit goes first). When it receives a group of non-8421 BCD entry, the output is R = 1. The system's state table after reduction is shown in Table 2. An initial state assignment SA0 using state variables (x, y, z) is scheme 1 in Table 3 with state set S = (A, B, C, D, E, F) and redundant state set RS = \{100, 101\}. From this state assignment the excitation functions of three flip-flops and the output function using SA1 can be extracted as follows:

\[
D_x = Txz + Tyz
\]

\[
D_y = z
\]

\[
D_z = y
\]

\[
R = Tx yz
\]

Now we discuss the multi-code assignment using algorithm 1.

Step 1: Because RS is not empty, define SAtemp to be SA0 and compute the occurrence probabilities of all the states in S based on Table 2 as follows.

Suppose a, b, c, d, e, f are occurrence probabilities of the six states A, B, C, D, E, F, and \( \tau \) is the probability of input variable \( T = 1 \). In line with the relationship between the present state and the next state, we have probability equalities as follows:

\[
a = e + f
\]

\[
b = a
\]

\[
c = b \cdot (1 - \tau)
\]

\[
d = b \cdot \tau
\]

\[
e = c \cdot (1 - \tau)
\]

\[
f = c \cdot \tau + d
\]

Take the first equality in eqn. 4 as example. From Table 2, we can find that the next state will be A if, only if the present state is E or F. Thus \( a = e + f \) is obtained. Other equalities in eqn. 4 are obtained analogously. From eqn. 4, we have

\[
a = b = c + d = e + f
\]

Furthermore, according to the normalisation of probability values, we have

\[
a + b + c + d + e + f = 1
\]
4 Conclusions

Since state assignment in the design of sequential circuits influences the complexity of combinational circuits, people attach importance to it in traditional design. In low power design, we find that the procedure of state assignment influences the state signal's switching behaviour during the state switching process. As the input to the combinational circuit, state variable lines have a close relation with the system's energy dissipation. Thus state assignment is an important research topic in low power design. Previous research has resulted in low power state assignment which would assign codes with minimum Hamming distances to states with high transition probabilities. This paper in contrast proposed state assignment which would exploit the redundant state codes to gate the clocks to some of the flip-flops. Multi-code state assignment not only eliminates the redundant state codes but also improves the system's reliability. An algorithm is hitherto proposed for the multi-code state assignment and three practical design examples show that this technique is feasible and can reduce energy dissipation.

5 Acknowledgment

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6 References

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