Technological Challenges of Advanced CMOS Processing and Their Impact on Design Aspects

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Abstract

The International Technology Roadmap for Semiconductors (ITRS) foresees the production of sub 10 nm gate length devices before 2016. To achieve this, both front- and back-end processing have to face major technological challenges and innovations. Lithography, device isolation, gate stack, shallow junctions, device engineering, high- and low-k dielectrics and interconnect schemes are hot research issues necessitating a global collaboration and the formation of appropriate platforms for joint research and development. Non-standard materials will have to be introduced and the use of non-classical device architectures will be required. This paper reviews some of the on-going research efforts to come to cost effective solutions forming the backbone for future technology nodes. Special attention is given to the impact of these technological innovations on design aspects. An outlook is also given of the emerging technologies that are at the basis of the switch over from micro- to nanoelectronics.

1. Introduction

The scaling of CMOS technologies aims at lowering the cost and increasing the performance and functionality of the circuits. According to Moore’s law, the number of transistors or memory bits is doubling every 1.5 to 2 years, and this trend is reflected in the International Technology Roadmap for Semiconductors (ITRS) [1]. This roadmap outlines the evolution of the different technology nodes and indicates the major technological challenges that will have to be faced. Figure 1 illustrates the evolution of the technology nodes for different applications, whereby it should be noticed that each update of the roadmap enhances the technology node by one year. The 90 nm technology is scheduled to be in production in 2004, while a decade later the 35 nm technology node should become available. By 2016, gate lengths as small as 9 nm should be manufactured. This acceleration of the ITRS roadmap imposes several technological challenges in order to avoid the so-called “Red Brick Wall”, i.e., technological areas for which no solution is available today and therefore requiring very innovative and high-risk research. This will go along with the introduction of new materials, as clearly illustrated by the study of the low- and high-k materials, and with the use of less standard manufacturing approaches. Typical examples are dry cleaning, atomic layer deposition, electroplating techniques, plasma and spike annealing etc.

Figure 1. ITRS roadmap (minimum linewidth versus year of production) for different type of devices and applications [1].

The overall optical lithography trend is going from 248 over 193 to 157 nm wavelengths. The implementation of resolution enhancement techniques such as phase shifting masks (PSM), off-axis illumination (OAI) and optical proximity correction (OPC) options will extend the lifetime of optical lithography and should lead to 65 nm geometries. The questions around the affordability of the lithography tools and the Cost of Ownership (CoO) are key issues from a manufacturing viewpoint. For the 45 nm and below technology nodes, however, the Next Generation Lithography (NGL), such as extreme ultraviolet lithography (EUV) operating at 13.5 nm wavelength, electron projection lithography (EPL), and X-ray lithography remain open. Optical lithography will not be further discussed in this paper and...
for a recent overview of the present state of the art reference is made to Van den hove et al. [2]. Although there are no direct physical and/or technological limitations for the near future, economical considerations will become of key importance for the selection of the lithography to be used.

For the different technology nodes the device isolation technique has to be optimized. This is not only posing technological difficulties, but has a strong impact on the design aspects. Therefore, both LOCOS based and shallow trench isolation will be briefly addressed.

Another key issue is the selection of the gate dielectric. Whereas the lifetime of SiO₂ can somewhat be extended by switching over to nitrided (NO) or reoxidized nitrided oxides (RNO), a further down scaling below the 65 nm node requires the implementation of high-k gate dielectrics such as e.g. ZrO₂, HfO₂, Al₂O₃, SrTiO₃, Ta₂O₅, TiO₂ and various silicate alloys. Both the fabrication techniques and reliability issues have to be investigated.

Device engineering is imposing major challenges for achieving the expected device performance. Novel concepts are introduced for controlling the channel profile, such as e.g. L-shape devices. Advanced ion implantation issues (e.g. use of BF₂ and In as dopants, new implantation techniques, reduced thermal budgets,…) are required for obtaining ultra shallow junctions. Also in the area of interconnects improved or novel silicidation techniques may have to be implemented. An area of extensive investigations is the back-end processing. Here process steps and modules such as low-k dielectrics, advanced metallization schemes (e.g. dual damascene), Cu metallization, and Chemical Mechanical Polishing (CMP) deserve full attention.

Investigations on non-classical alternative CMOS structures and new architectural concepts, such as e.g. vertical transistors, double-gate devices, band gap engineered transistors and the use of ultra-thin silicon-on-insulator concepts, are extensively investigated.

The paper first outlines some basic concepts related to the impact of scaling on the device performance, before addressing more in detail some of the future technological challenges. Some of the above mentioned topics are discussed in order to illustrate how deep submicron technologies can be realized. Finally the future outlook is addressed, including the transition area between micro- and nano-electronics.

2. Downscaling and device performance

The competitiveness of the IC market necessitates an increased functionality and device performance for a reduced cost per function. The scaling MPU requirements are more stringent for MPUs than for DRAMs. However, the aggressive trend in downscaling will not continue and several performance parameters will rather saturate, such as e.g. the MPU clock frequency at 3 GHz which will be limited by the on chip propagation of the electromagnetic waves and the dielectric constant of the used materials [3].

Scaling of the supply voltage has a beneficial impact on the gate dielectric leakage, the junction breakdown and the latch-up performance [4]. There is also an influence on the transistor drive current $I_{DSAT}$, which is given by the formula:

$$I_{DSAT} \approx \frac{\varepsilon_{ox} \mu W}{EOT} \frac{(V_{GS} - V_T)^\gamma}{L_{eff}}$$

where $\varepsilon_{ox}$ is the dielectric constant, $\mu$ is the carrier mobility, $W$ is the device width, $T_{EOT}$ is the equivalent gate oxide thickness, $L_{eff}$ is the electrical device length, $V_{GS}$ is the gate voltage, $V_T$ is the threshold voltage and $\gamma$ is a parameter between 1 and 2. The scaling of the supply voltage $V_{DD}$ and the $V_{DD}/V_T$ ratio lowers the gate overdrive voltage. The electron mobility decreases by reducing the effective gate length and is dominated by surface scattering. An increase of the $\varepsilon_{ox}/T_{EOT}$ ratio has a positive influence on the drive current. The drive current on itself is limiting the gate delay, as both parameters are linked by the expression

$$t_{pd} = C_{gate} \frac{V_{DD}}{I_{DSAT}}$$

with $C_{gate}$ the gate capacitance. In case the original scaling method (constant electric field) proposed by Dennard et al. [5] is used, a reduction of the device length with a factor $K$ will reduce both the drive current and the gate delay with a factor $1/K$. The downscaling of the devices also requires a suppression of short channel effects and an optimization of the channel and source/drain resistances, so that in practice different scaling rules are applied [43,6]. The high-performance devices are the technology driver, with as target to reach an average 17% per year improvement in gate delay.

3. Ultimate CMOS technology challenges

3.1 Device isolation

The LOCal Oxidation of Silicon (LOCOS) technique has since its invention in 1970 [7] extensively been used as the key device isolation approach. Optimization of the LOCOS parameters (e.g. pad oxide and nitride thickness, field oxidation ambient and temperature, implementation of a polysilicon layer, etc) allows minimizing the bird’s beak (BB) length so that design rules remain adequate for 0.35 μm technologies. Beside the BB length, attention has also to be given to possible defect generation in the silicon substrate due to mechanical stress. The Poly Encapsulated LOCOS (PELOX) technique can be used for 0.25 μm circuits [8]. However, for sub-0.25 μm
CMOS the only viable approach coping with the requirements in terms of active area scaling and planarity at gate level is shallow trench isolation (STI). Differences between LOCOS and STI are clearly illustrated in Fig. 2.

![LOCOS and STI](image)

Figure 2. SEM micrographs of LOCOS and STI based isolations, showing the differences in bird’s beak length and planarity.

Although good planarization is obtained with CMP after the trench filling, problems remain with the pattern density dependent polishing rate, possible dishing effects in field regions, and erosion of the nitride layers covering the active areas. A commonly used approach is to implement dummy active area regions, designed in such a way that a good uniformity is obtained of active areas over the chip and over the wafer. This works nicely for digital circuits, but in the case of mixed signal applications the increased capacitive coupling and the noise associated with routing traversing dummy structures may become problematic, especially when the dummy areas are automatically generated once the design has been finalized. To overcome this problem, a dummy free STI approach, called the dual nitride concept, has been reported [9]. The concept is based on the implementation of a protective nitride layer on top of larger field regions in addition to the use of a polishing slurry with a high density dependent polishing rate, possible dishing effects in field regions, and erosion of the nitride layers covering the active areas. A commonly used approach is to implement dummy active area regions, designed in such a way that a good uniformity is obtained of active areas over the chip and over the wafer. This works nicely for digital circuits, but in the case of mixed signal applications the increased capacitive coupling and the noise associated with routing traversing dummy structures may become problematic, especially when the dummy areas are automatically generated once the design has been finalized. To overcome this problem, a dummy free STI approach, called the dual nitride concept, has been reported [9]. The concept is based on the implementation of a protective nitride layer on top of larger field regions in addition to the use of a polishing slurry with a high density dependent polishing rate, possible dishing effects in field regions, and erosion of the nitride layers covering the active areas.

### 3.2 Gate dielectrics

Scaling has direct consequences for the gate dielectric of the transistor. Standard SiO$_2$ as thin gate dielectric faces several difficulties such as; i) for a too low thickness the reproducibility and uniformity of the fabrication process decrease, ii) no longer sufficient resistant to the in-diffusion of boron from the p$^+$-doped polysilicon [10], iii) reliability restrictions, especially for slightly higher operating temperatures [11], iv) reduced hot carrier immunity, v) direct tunnelling, with an exponential increase of the tunnel current [12], vi) quantum mechanical effects [13]. For the 90 nm technology node the $T_{EOT}$ is about 0.9-1.4 nm, implying that the direct tunnelling gate leakage current becomes of the same order as the device off current, thereby impacting the off-state power level of the devices. Therefore, much attention is given the use of high-$k$ dielectrics as a replacement [14], allowing a thicker dielectric film according to the formula

$$ T_{dielectric} = \frac{k_{dielectric}}{k_{ox}} T_{ox} $$

The selection of the high-$k$ material has to account for thermal stability during the CMOS processing, compatibility with the selected gate material (polysilicon, polycides or metal) and manufacturing and yield aspects [15]. The stringent requirement of 1 pA/mm on the gate leakage current in the standby mode will already around 2005 require the use of high-$k$ dielectrics. Later, these will be implemented in the high-performance chips.

A first step to increase the dielectric constant is the implementation of nitrided oxides (NO) or reoxidized nitrided oxides (RNO). Nitrogen incorporation in the oxide provides a good barrier against dopant diffusion, leads to an increase of the dielectric constant, and has a beneficial impact on the reliability [16-17]. However, as there is less than a factor of two increase in the dielectric constant compared to oxide, the used film thickness must remain rather thin to obtain the required capacitance. In most cases these films are operating in the direct tunnelling region, whereby the tunnel current increases monotonically with the oxygen content for a given equivalent oxide thickness [18]. Another important aspect is the low frequency noise performance of nitrided oxides [19]. This is illustrated in Fig. 3, showing the normalized input referred voltage noise spectral density as a function of the square of the oxide thickness for three CMOS generations [20]. Only for 0.18 μm CMOS NO is used, resulting in an increase of the noise of the PMOS devices. A reoxidation of the NO oxide reduces the noise due to a shift of the N-profile further away from the Si interface. The noise performance is determined by both the nitrogen concentration and its peak location in the dielectric [19].

![Normalized input-referred voltage noise spectral density](image)

Figure 3. Normalized input-referred voltage noise spectral density as a function of the oxide thickness for three CMOS generations: 0.35 ($t_{ox}$=6.5 nm), 0.25 ($t_{ox}$=5 nm) and 0.18 μm ($t_{ox}$=3.5 nm NO or RNO). $V_{GS}$=1 V, $V_{DS}$=0.1 V. For the 0.18 μm node NO annealed oxides are considered as standard. (After Da Rold et al. [20]).
The feasibility of using alternative high-$k$ gate dielectrics such as e.g. Sc$_2$O$_3$ ($k>10$), Ta$_2$O$_5$ ($k=25$), TiO$_2$ ($k=60$), and BST ($k=300$) is getting much attention. Although it is not clear yet who will be the winner, very promising results have already been published for a variety of dielectrics such as HfO$_2$ [21-22], TiO$_2$/Si$_3$N$_4$ dielectrics [23] and La$_2$O$_3$ [24] respectively. A comparison of the gate leakage current for different high-$k$ materials in respect to SiO$_2$ is given in Fig. 4 [25]. The hafnium oxides have a higher thermal stability over zirconium oxide, and the addition of silicon and aluminium has a beneficial impact in relation to recrystallization. It is quite important to obtain good interfacial properties between the high-$k$ dielectric and both the silicon substrate and the polysilicon gate electrode. For the first interface a thin SiO$_2$ layer is often grown first, but at the expense of the composite dielectric constant. The top interface remains a challenge [26] even in case that a metal gate electrode is used.

Figure 4. The gate current density at 1 V for different high-$k$ dielectrics in comparison to SiO$_2$.(After Iwai [25]).

The reduction in the effective gate dielectric thickness leads to an increase of the capacitance resulting from the depletion layer in the polysilicon. Therefore, more and more attention is given to the use of metal gates in combination with high-$k$ dielectrics. These metals must have appropriate work functions and should be thermally stable with respect to oxidation and phase changes.

It is important to keep in mind that by the use of heavy metal oxides and silicates, such as e.g. ZrO$_2$, HfO$_3$, HfSiO$_2$ and HfSiO$_4$, metals may diffuse into the silicon and degrade the electrical properties. Especially Zr and Hf have a relative high diffusivity and will introduce different trapping levels in the band gap [27].

Also in the case of high-$k$ dielectrics it is important to investigate the impact of the gate dielectric on the low frequency noise performance. So far only limited data has been reported on the $1/f$ noise performance of these materials [19]. However, the data reported on both HfO$_2$ [28] and La$_2$O$_3$ [29] are promising. Figure 5 shows the $1/f$ performance of HfO$_2$ [28]. Based on the LF noise theory, it can be concluded that there is a high bulk trap density. For the moment, it has been observed that for these materials there is a roughly 50 times highly trap concentration in the dielectric compared to SiO$_2$, explaining the higher noise figure.

Figure 5. Low frequency noise performance of n-MOS HfO$_2$ devices.

3.3 Device Engineering

The scaling of the lateral and vertical transistor dimensions imposes severe challenges to the overall device engineering approach, i.e., shallow junctions, channel profile control, spacer concepts, source/drain extensions, etc.

The control of the dopant profiles requires a tight control of the overall thermal budget during processing, without penalizing the dopant activation and the elimination of the ion-implantation damage. Several optimized Rapid Thermal Anneal (RTA) schemes have been proposed [30]. Dependent on the ramp rate and the doping type, the profiles may be degraded due to transient enhanced diffusion (TED) in addition to the possible negative impact of the defect growth during the ramp-up cycle. As TED is caused by the excess interstitials generated by the ion implantation damage, defect engineering can be used for TED suppression [31]. A lower implant energies aggravates TED and reduces the dopant activation [32]. Atomic layer doping is a promising technique for sub 20 nm junction depths [33].

The silicidation process has an impact on the junction depth (through the consumption of silicon) and the junction leakage. For sub 65 nm technology nodes NiSi is a strong candidate to replace CoSi$_2$ [34]. The silicide selection has to take account aspects such as the series resistance, the thermal stability, the junction leakage, the yield and the tolerable process window. An optimized Ni silicidation process achieves similar series resistances as for CoSi$_2$, but requires a lower thermal budget and enables the silicidation of narrow lines [35].

Highly doped shallow junctions can be fabricated by e.g. low-energy implants, plasma doping and/or the use of selective epitaxy. Selective CVD of boron or phosphorous doped SiGe leads to recessed regions with a well
controlled shallow junction depth and allow to optimise parameters such as contact resistance, series resistance and junction abruptness [36]. The strain associated with the pseudomorphic SiGe allows achieving higher concentrations of active boron than in the case of ion implantation in silicon, thereby reducing the contact resistivity. Device engineering based on lowly doped drain (LDD) regions, source/drain extensions, HALO or highly doped drain (HDD) regions are well-known approaches and all require a very tight control of the thermal budget [37]. Recently, a L-shaped spacer architecture has been proposed in order to reduce the minimal spacing between adjacent spacers. As nitride L-shaped spacers are formed before extension and junction implants, the process complexity is reduced by elimination of lithographic and implantation steps and reducing the total thermal budget [38]. Compared to standard D-shape spacers, these spacers allow to relax on the gate electrode thickness while establishing a good device performance, a good immunity to silicide bridging and enabling to increase the packing density [39]. The sheet resistance of active areas between two neighboring spacers as function of the space to spacer distance is shown in Fig. 6 for a Co silicide with a Ti capping layer, illustrating the good performance of L-shape spacers.

Figure 6. Sheet resistance of a common transistor source-drain as a function of the spacer to spacer distance. (after Augendre et al. [39]).

3.4 Interconnects and Multilevel Metallization

Scaling has strongly improved the transistor speed-power product, but has also increased the interconnection impedance by raising both the resistance of the metal lines and their capacitive coupling. The improved gate delay can only beneficially be used in integrated circuits if also the interconnect delay is minimized. Therefore the so-called back-end of line (BEOL) processing, i.e. intermediate layer dielectrics (ILDs), metallization schemes, intermetal dielectric layers (IMDs) and multilevel metallization systems, has received much attention is nowadays the most time consuming and expensive part of the processing. Directly associated with this issue is the use of oxide and metal CMP in order to achieve the required depth of focus (DOF) for the optical lithography.

A large variety of low-\(k\) dielectrics are investigated as potential candidates [40]. Early winners include hydrogen silsesquioxane (HSQ) and fluorinated oxides resulting in a \(k\)-value of 3 and 3.5 respectively. For lower \(k\)-values, organic polymers such as poly(arylene)ethers (PAE), benzocyclobutene (BC) and an aromatic hydrocarbon have been studied. Also silicon based CVD films are very promising. In case that ultra-low \(k\)-values are needed, spin-on candidates include nanoporous silica films, porous polymers and polytetrafluoroethylene (PTFE). Beside the deposition technique (CVD, spin-coating...) attention has to be given to the dry etch performance and to the planarization (locally and global) aspects.

Another important issue is the metallization approach, e.g. single or dual damascene, and the choice of the metallization system, such as e.g. hot Al or Cu. The selected solution must take into account issues such as seed layers, barrier layers (TiN, TaN, CVD-WN...), the type of fill process (Cu deposition, electroless deposition, electroplating), dry etch aspects, CMP performance, overall manufacturability and CoO.

4. Beyond classical CMOS

Devices with 9 nm gate length will be in production not later than 2016. However, the 2001 ITRS update is also scheduling so called Emerging Research Devices. Some of these devices will be briefly discussed.

Silicon-on-Insulator (SOI) technologies offer improved device performance. Compared to bulk Si, SOI CMOS can run at 20 to 50% higher switching speeds or with a 2 to 3 times lower power consumption for the same speed [41-42]. In contrast to bulk devices, ultra-thin SOI doesn’t require an increase of the doping level, thereby allowing achieving higher channel mobilities. The use of a ground-plane underneath the thin buried oxide and/or the implementation of a thin buried high-\(k\) dielectric can suppress fringing field effects [43].

Both fully and partially depleted technologies are used. Ultra-thin film FD devices have an improved sub-threshold slope and a better threshold voltage controllability. The main challenges are the control of the thin film thickness, the gate stack scaling and the elimination of short-channel effects.

There is also much interest in using multiple gate structures (Fig. 7), with 2, 3 or 4 gates [44]. Compared to single gate structures, these devices offer much better...
control of short channel effects (SCE) and an enhanced current drive capability. Although the surrounding gate structure is the best in terms of subthreshold swing, current drive and drain induced barrier lowering (DIBL), triple gate structures are easier to implement.

Figure 7. Schematic illustration of single and multiple gate structures on SOI substrates. (after Colinge [43]).

Much research activities are concentrating on the so-called FinFET approach. A FinFET is a double-gate transistor having surface conduction channels on two opposite vertical surfaces, whereby the current is flowing in the horizontal direction. The channel length is determined by the horizontal separation between source and drain and is usually controlled by a lithographical step combined with a sidewall spacer etch process. The feasibility of 27 nm gate length SOI devices has already been demonstrated [44]. The main advantages are a higher drive current, improved sub-threshold slope and suppressed short-channel effects. Other type of double-gate structures with surface conduction channels on two opposite horizontal surfaces and having a current flow in the horizontal direction are being investigated [45]. The channel length is controlled in a similar way as for the FinFET. The device performance of FinFETs depends on the processing, which may increase the surface roughness after etching the silicon Fins, and can be improved by a hydrogen annealing step before the gate oxidation [46]. The beneficial impact of a 900°C thermal anneal on the low frequency noise is illustrated in Fig. 8.

Band-gap engineering allows increasing the mobility of the carriers in the channel without changing the physical structure of the transistor. Major efforts are concentrating on SiGe or strained Si on a relaxed SiGe layers for both bulk and SOI technologies [47-48]. The introduction of Si$_{0.7}$Ge$_{0.3}$ in the channel of thin-film SOI devices resulted in a 70% enhancement of the drive current of 50 nm p-MOSFETs [49]. The addition of carbon to the SiGe layers offers benefits with respect to strain relaxation, the diffusion control of dopants and improved device characteristics [50].

Non-classical CMOS approaches also include vertical transistors, having surface conduction channels on two or more vertical surfaces and current flowing in the vertical direction [51]. The channel length is determined by the vertical separation between source and drain and is usually controlled by an epitaxial layer instead of by a lithographical step. The vertical scaling of layers down towards atomic dimensions may be overcome by the introduction of new materials. However, the horizontal scaling leads to quantum mechanical effects in the current transport in the channel and enhanced tunneling effects between source and drain. The ultimate CMOS scaling limit is around 5 nm for room temperature operation [52].

Figure 8. Impact of a pre-gate oxidation hydrogen anneal step on the average equivalent noise versus frequency in CMOS FinFETs biased at $I_d = 2 \, \mu A/\mu m$. (After Lee et al. [46]).

Nanoelectronics consists of a new family of devices and components such as single electron transistors (SETs), resonant tunnelling diodes (RDTs), spin controlled devices or so-called spintronic, rapid single quantum flux logic (RSFQ), and intramolecular nanoelectronics. SETs can be considered as devices making a bridge between micro- and nanoelectronics. However, they are not yet a mature alternative to CMOS because of some remaining challenges [53] such as there are i) controlling the background charges, ii) reproducibility and manufacturing tolerances, iii) electrostatic interactions between the devices, iv) control of the operating conditions such as voltage range and temperature, and v) some technological bottlenecks.

An important emerging field is based on fullerenes and carbon nanotube devices [54] A carbon nanotube is a molecular tube or cylinder formed from an atomic sheet of carbon atoms, bonded together into an array of hexagons, which is rolled up to a tube. The tubes can be doped n- or p-type enabling the formation of p-n junctions. Several components such as SETs, field-effect transistors, junction devices and charge-storage memory devices have already been fabricated [55].

Another interesting issue is the impact of systems on a chip (SOCs) on the ITRS roadmap. The SOCs may even include combinations with molecular devices. Although this may relax some of the present challenges, new ones are associated with the intra- and interchip interconnects and package aspects. There is also a strong tendency to increase the functionality with process options such as
e.g. non-volatile memories (FeRAMs and MRAMS), rf-technologies based on SiGe or SiGeC strained layers in CMOS or BiCMOS.

References


28. E. Simoen, A. Mercha, L. Pantisano, C. Claeys and E. Young, 
*Second Int. Symp on High Dielectric Constant Materials*, 
abstract nr. 223.
29. H. Saudinn, Y. Yoshihara, S. Ohmi, K. Tsutsui and H. Iwai, 
*Second Int. Symp on High Dielectric Constant Materials*, 
abstract nr. 712.
30. L.A. Larsen and B.C. Covington, Shallow junction challenges 
to rapid thermal processing. In *Rapid Thermal Processing 
and Other Short-Time Processing Technologies*, ed. by F. 
Roozboom, M. C. Oztruk, J. C. Gelpey, K. G. Reid and D.-L. 
Kwong (The Electrochem. Soc., Pennington) PV 2000-09 
31. V. Privitera, Impact of the purity of silicon on the evolution 
of ion beam generated defects: From research to technology. In 
*High Purity Silicon VI*, ed. by C. L. Claeys, P. Rai- 
Choudhury, M. Watanabe, P. Stallhofer and H. J. Dawson 
606-620.
32. A. Nishida, E. Murakami and S. Kimura, Characteristics of 
low-energy BF2- or As-implanted layers and their effect 
on the electrical performance of 0.15 μm MOSFETs. 
33. M. Koyanagi, Ultra-shallow junction formation by atomic 
layer doping. In *ULSI Process Integration II*, ed. by C. 
Claeys, F. Gonzalez, H. Murota and K. Saraswat (The 
34. Q. Xiang, NiSi salicide for sub 100 nm CMOS. In 
*Semiconductor Silicon 2002*, ed. by H.R. Huff, L. Fabry 
and S. Kishino (The Electrochem. Soc., Pennington) 2002-02 
35. B. Froment, M. Muller, H. Brut, R. Pantel, V.Carron, H. 
Achard, A. Halimaoui, F. Boeuf, F. Wacquant, C. Regneir, D. 
Ceccarelli, et al., Nickel vs. Cobalt silicide integration for 
sub-50 nm CMOS. In *Proc. ESSDERC 2003*, ed. By J. Franca 
36. M.C. Oztruk, N. Presovic, J. Liu, H. Mo, I. Kang and S. 
Gannavaram, A new junction technology based on selective 
CVD of SiGe alloys for CMOS technology nodes beyond 30 nm. In 
*Semiconductor Silicon 2002*, ed. by H.R. Huff, L. Fabry 
and S. Kishino (The Electrochem. Soc., Pennington) 2002-02 
37. H. Wakabayashi, M. Ueki, M. Naritomo, K. Uejima, T. Fukai, 
M. Togo, T. Yamamoto, K. Takeuchi, Y. Ochiai and T. 
Mogami, Process technology for sub 100-nm CMOS devices. In 
*ULSI Process Integration II*, ed. by C. Claeys, F. 
Gonzalez, J. Murota and K. Saraswat (The Electrochem. Soc., 
38. E. Augendre, C. Perello, E. Vandamme, S. Pochet, R. 
Rooyackers, S. Beckx, M. de Potter, A. Lauwers and G. 
Badenes, L-shape spacer architecture for low cost, high 
performance CMOS. In *ULSI Process Integration II*, ed. by C. 
Claeys, F. Gonzalez, J. Murota and K. Saraswat (The 
39. E. Augendre, R. Rooyackers, M. de Potter de ten Broeck, E. 
Kunnen, S. Beckx, G. Mannanert, C. Vrancken, V. Vassilev, T. 
Chiarella, M. Jurczak and I. Debuisschere, Thin L-shaped 
40. H.S. Nalwa, Handbook on low and high dielectric constant 
materials and their applications – Materials and processing, 
41. D.K. Sadana, SOI for CMOS logic and memory applications. 
In *ULSI Process Integration II*, ed. by C. Claeys, F. 
Gonzalez, J. Murota and K. Saraswat (The Electrochem. Soc., 
42. S. Cristoloveanu, SOI technology: The future will not scale 
Fabry and S. Kishino (The Electrochem. Soc., Pennington) 
43. J.P. Colinge, Multiple gate silicon-on-insulator MOS 
– SBMICRO 2003*, ed. by J.A. Martino, M.A. Pavanello 
and N.I. Morimoto (The Electrochem. Soc., Pennington) 2003-09 
Asano, C. Juo, E. Anderson, T.-J. King, J.Bokor and C. Hu, 
FinFET – A self-aligned double-gate MOSFET scalable to 20 nm. 
45. F. Allibert, T. Ernst, J. Pretet, N. Hefyene, C. Perret, A. 
Zaslavsky and S. Cristoloveanu, From SOI materials to 
559-566.
46. J.-S. Lee, Y.-K. Choi, D. Ha, S. Balasubramanian, T.-J. King 
and J. Bokor, Hydrogen annealing effect on DC and low- 
frequency noise characteristics in CMOS FinFETs. *IEEE 
47. J. Aliue, T. Skotnicki, P. Bouillon, J.L. Regollini, A. Souifi, 
G. Guilot and G. Bremond, Potential of SiGe channel 
MOSFETs for a submicron CMOS technology. In *Future 
trends in microelectronics*, ed. S. Luryo, J. Xu and A. 
48. S. Tagai, T.Mizuno, N. Sugiyama, T. Tezuka and A. Kurobe, 
Strained Si on insulator (strained SOI) MOSFETs – 
Concepts, structures and device characteristics. *IEICE Trans. 
49. Y.-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T.-J. 
King, J. Bokor and C. Hu, Design and fabrication of 50 nm 
thin-body p-MOSFETs with a SiGe heterostructure channel. 
50. H.J. Osten, SiGeC device applications. In *Semiconductor 
Silicon 2002*, ed. by H.R. Huff, L. Fabry and S. Kishino (The 
51. K. De Meyer, N. Collaert, S. Kubicek, A. Kottantharayil, H. 
van Meer and P. Verheyen, Emerging device solutions for the 
by C. Claeys, F. Gonzalez, J. Murota, P. Fazan and R. Singh 
52. H. Kawaura and T. Sakamoto, Electrical properties of 
by H.R. Huff, L. Fabry and S. Kishino (The Electrochem. Soc., 
van Meer and P. Verheyen, Emerging device solutions for the 
by C. Claeys, F. Gonzalez, J. Murota, P. Fazan and R. Singh 
54. H.S. Nalwa, Handbook on low and high dielectric constant 
materials and their applications – Materials and processing, 
55. D.K. Sadana, SOI for CMOS logic and memory applications. 
In *ULSI Process Integration II*, ed. by C. Claeys, F. 
Gonzalez, J. Murota and K. Saraswat (The Electrochem. Soc., 